PDP-11/70 panel behaviour research at LCM
Feb 12th 2018
RESULTS

Mike Hill, mike.hill@pogiot.com
Jörg Hoppe, j_hoppe@t-online.de
Oscar Vermeulen, oscar.vermeulen@hotmail.com

LCM Support:
Rich Alderson, RichA@LivingComputerMuseum.org
Josh Dersch, JoshD@LivingComputerMuseum.org

Onsite

Unzip BLINKY_rp06.zip to create BLINKY_rp06.dsk (you may test this at home). Map this file using the disk emulator to an RP06 unit.

Mounting the image caused problems. Rich Alderson had to login to the RP drive simulator. Due to a bug on LCM side the BLINKY image was permantly unmounted. Rich also sat far away from 11/70.

Boot the 11/70 from the emulated RP06 disk unit.
Start M9312 monitor:
Switches=1765020, LOAD ADR, START. On „$" prompt: „DB"

At this point, BLINKY is running and the LEDs are bouncing.

SCRIPT USAGE

At the start of each script, the ADDR knob should be on PROG PHY and the DATA knob should be on DATA PATHS and all switches in the switch register should be off (SWR=000000).

Most of the scripts expect BLINKY to be either running or in memory.

The later scripts overwrite bits of BLINKY's code, so if you mess up you might need to reboot BLINKY.

Script 0 – machine check

[ ] LAMP TEST on machine

Photo: TB8A3108

Movie: TB8A3105

PDP-11/70 „Miss Piggy“ has abnormal SR switches:
SW 21-18 are 0 in low position, and 1 in middle positions.
SW 17-0 are 0 in middle position and 1 in up position, as usual.
SO if all SR are optical in line, the value is 17000000 !

Script 1 - BASELINE

Run BLINKY.
Each row of LEDs should "bounce" in a similar fashion.
Especially on the top row U with 22, S with 18 and K with 16.

[ ] Is RUN   on steadily [X] or flashing? [ ]
[ ] Is PAUSE on steadily [ ] or flashing [ ] or off? [X]
[ ] Is MASTER on steadily [ ] or flashing [ ] or off? [X]
[ ] Is DATA   on steadily [ ] or flashing [ ] or off? [X]
[ ] While running: ADDR select all 8 positions. DATA SEL all 4 positions.

Movie: TB8A3109

Script 2 - PARITY LEDS

Observe the PARITY LEDs:

[ ] 00 - Odd parity on last memory reference from an instruction
[ ] 01 - Even parity on instruction fetch (WAIT=000001)
[ ] 10 - Odd parity on instruction fetch (WAIT=000001)
[ ] 11 - Even parity on last memory reference from an instruction

Just observe. The parity LEDs are based on memory accesses and should match the high/low byte of the DATA LEDs if the data came from main memory (0=LED off, 1=LED on).

Movie: TB8A3110

Data from addr 0 was examined

Addr	word	high	low	Par H	Par L
000000	000240	000	240	1	1
000002	000412	001	012	0	1
000006	000357	000	357	1	0
000022	011600	430	200	0	0

=> even number of bits => Parity = 1

Movie: TB8A3112 single step execution

Script 3 - LEDS when SELECTOR SWITCHES ROTATED

Switch each of the knobs to all possible positions to see the effects on the ADDR LEDs (BLINKY does not enable separate D space) and DATA LEDs.

Movie: TB8A3113

Script 4 - DATA LEDS WHEN BUS REG SELECTED

[During this test, we only write one word to I/O space (177570 = Display Register) per second.]

Switch the DATA knob to BUS REG.
Observe the DATA LEDs and PARITY LEDs.

The 1 I/O per second is to say that this will NOT affect the test. We are interested in whether anything else is seen.

Movie: TB8A3114

Script 5 - DATA LEDS when MOVING TO FROM/TO I/O SPACE

[This test uses byte reads/writes from/to I/O space (the console I/O buffers)]

For scripts 5 & 6:

Leave/set ENABLE/HALT at/to HALT
Deposit at 00000040 : 105737 [TSTB @#x   ]
Deposit at 00000042 : 177560 [177560   ]
Deposit at 00000044 : 100375 [BPL 000040]
Deposit at 00000046 : 000766 [BR 000024]

Set SWR=00000040
Press LOAD ADRS
Set ENABLE/HALT to ENABLE
Press START
Press any key on the DECWRITER to halt the test (or switch ENABLE/HALT to HALT)

THE FOLLOWING TEST WAS NOT EXECUTED: MACHINE HALTED, SO NO RESPONSE ON KEY PRESS. WE SHOULD HAVE STARTED EXECUTION AT 0040, BUT DID NOT UNDERSTOOD THAT IN FIELD TEST SITUATION:
„At the console, constantly press any repeating character e.g. 'S' and observe the DATA LEDs and PARITY LEDs again.

You can see them in REALCONS (but I don’t think you should be able to).“

Movie: TB8A3115

Script 6 - BUS REG LEDS when MOVING TO FROM/TO I/O SPACE

[This test uses byte reads/writes from/to I/O space (the console I/O buffers)]

For scripts 5 & 6:

Leave/set ENABLE/HALT at/to HALT
Deposit at 00000040 : 105737 [TSTB @#x   ]
Deposit at 00000042 : 177560 [177560   ]
Deposit at 00000044 : 100375 [BPL 000040]
Deposit at 00000046 : 000766 [BR 000024]

Set SWR=00000040
Press LOAD ADRS
Set ENABLE/HALT to ENABLE
Press START
Press any key on the DECWRITER to halt the test (or switch ENABLE/HALT to HALT)

THE FOLLOWING TEST WAS NOT EXECUTED: MACHINE HALTED, SO NO RESPONSE ON KEY PRESS. WE SHOULD HAVE STARTED EXECUTION AT 0040, BUT DID NOT UNDERSTOOD THAT IN FIELD TEST SITUATION:

„Switch the DATA knob to BUS REG.
At the console, constantly press any repeating character e.g. 'S' and observe the DATA LEDs and PARITY LEDs again.“

Movie: TB8A3116, TB8A3117

Script 7 - TEST LOAD ADRS + START

Switch ENABLE/HALT to HALT (and leave it there)
Note down the address in the ADDR LEDs (the CONT address)
Set SWR=00000002
Press LOAD ADRS then START then CONT
[ ] Do the ADDR LEDs show 000000002? Don't expect this
[X] Do the ADDR LEDs show 000000030? Means LOAD ADDR+START sets PC and RESETs
[ ] Something else? [_____] Means LOAD ADDR only RESETs

Movie: TB8A3118

Script 8 - TEST CONSOLE ADRS ERR LED

Leave/set ENABLE/HALT at/to HALT
Set SWR=17777754
Press LOAD ADRS
Press and hold down EXAM
[ ] What LEDs are lit on the ADDR and DATA LEDs?
„ADRS ERR" ON, ADR switches to 17600000!
Let the EXAM switch go
[X] Is the ADRS ERR LED on?
Set SWR=00000000
Press LOAD ADRS then EXAM
[ ] Is the ADRS ERR LED (still) on?
LOAD ADR clears ADRS ERR
If the ADRS ERR LED is still on, press START
[ ] Is the ADRS ERR LED off now?

Movie: (TB8A3119), TB8A3120

Another EXAM on the changed 17600000 remains in ADR ERR, as „Miss Piggy" probably has less then 4M memory installed.

Script 9 - TEST CONSOLE ACCESS TO REGISTERS

Leave/set ENABLE/HALT at/to HALT
Set SWR=17777674 (MMU PAR)
Press LOAD ADRS then EXAM / EXAM / EXAM
1. EXAM: ADDR= 17777674, DATA=06137, ADRS ERR OFF
2. EXAM: ADDR= 17777676, DATA=06137, ADRS ERR OFF
3. EXAM: ADDR= 17777674, DATA=06137, ADRS ERR ON
4. EXAM: ADDR= 17777674, DATA=06137, ADRS ERR ON ?
[ ] What do the ADDR LEDs show?
[ ] Is the ADRS ERR LED on?
If the ADRS ERR LED is still on, press START (RESET)
ADDR= 177674

Movie: TB8A3121

So EXAM STEP is disabled, when ADRS ERR = ON

Script 10 - TEST 'WAIT' INSTRUCTION DISPLAYS R0

BLINKY rebootet

Leave/set ENABLE/HALT at/to HALT
Deposit at 00000422 : 000002 [RTI] ; Avoids memory reference
Deposit at 00000674 : 000240 [NOP]
Deposit at 00000676 : 012300 [MOV (R3)+,R0]

Set SWR=00000000
Press LOAD ADRS
Set ENABLE/HALT to ENABLE
Press START
[X] Do the DATA LEDS still show a bouncing pattern? (YES = WAIT shows R0)

Movie: TB8A3123

Anomaly: After SWR=674 LOAD ADR, ADDRESS shows 574 ! But selector is PROG PHY, should be CONS PHY. Deposit into 574 should change MMU pattern, but this is undisturbed => indeed 674 changed.

Script 11 - TEST ADRS ERR LED & 'HALT' SHOWS R0

```
Leave/set ENABLE/HALT at/to HALT
Deposit at 00000070 : 012700 [ MOV (PC)+,R0 ]
Deposit at 00000072 : 177754 [ 177754       ]  ; Cause UNIBUS timeout
Deposit at 00000074 : 005710 [ TST (R0)     ]

Set/leave ENABLE/HALT to/at ENABLE
Press CONT & wait for a few seconds

Press any key on the console keyboard once
[ ] Is the ADRS ERR LED on?          (Should be)
[X] Do the ADDR LEDS show 00000026?  (Should do)
[X] Do the DATA LEDS show   000076?  (YES = HALT shows R0)

Press CONT
[ ] Is it still on?  (Might be if clearing it is under program
control: MSER) (ADRS ERR not ON)

Set SWR=00000000
Press START
[X] Is the ADRS ERR LED off?


Program HALTs on keypress. ADRS ERR LED not ON.

Movie: TB8A3128
```

Script 12 - FURTHER TEST OF WHAT DATA PATHS SHOW

Only perform this script after script 11 is complete (WHY?)
Leave/set ENABLE/HALT at/to HALT
Deposit at 00000070 : 000777 [BR .]

Set/leave ENABLE/HALT to/at ENABLE
Press CONT & wait for a few seconds
HIT DECWRITER KEY TO STOP
SWITCH DATA SEL TO „BUS REG“

[X] Do the DATA LEDS show 000777? (YES = DATA LEDS show instruction stream)

Movie: append TB8A3129 and TB8A3130

Script 13 - ANOTHER TEST OF WHAT DATA PATHS SHOW

Only perform this script after script 11 or 12 is complete
Leave/set ENABLE/HALT at/to HALT
Deposit at 00000070 : 000167 [JMP x(PC)]
Deposit at 00000072 : 177774 [x=000070]

Set/leave ENABLE/HALT to/at ENABLE
Press CONT & wait for a few seconds
HIT DECWRITER KEY TO STOP

[ ] Do the DATA LEDS show 177774? (YES = DATA LEDS show instruction stream)
[X] Something else? [all LEDs active, as probably mix of 000167 and 177774 is displayed]

Movie: TB8A3131

Script 14 - TEST 'RESET' INSTRUCTION DISPLAYS R0

```
Leave/set ENABLE/HALT at/to HALT
Deposit at 00000040 : 005200 [ INC R0    ]
Deposit at 00000042 : 000005 [ RESET     ]
Deposit at 00000044 : 000775 [ BR 000040 ]

Set SWR=00000040
Press LOAD ADRS
Set ENABLE/HALT to ENABLE
Press START
[X] Do the DATA LEDS show a quickly increasing number? (YES = RESET
shows R0)


Movie: TB8A3132
```

Script 15 - WHICH REGISTER SET IS USED FOR 'HALT' DISPLAY R0 ?

```
Leave/set ENABLE/HALT at/to HALT
Deposit at 00000040 : 012700 [ MOV #x,R0  ]
Deposit at 00000042 : 004340 [ RS1 + PR7  ]
Deposit at 00000044 : 010037 [ MOV R0,@#x ]
Deposit at 00000046 : 177776 [ PSW        ]
Deposit at 00000050 : 005000 [ CLR R10    ]
Deposit at 00000052 : 000764 [ BR 000024  ]

Set SWR=00000040
Press LOAD ADRS
Set ENABLE/HALT to ENABLE
Press START
[ ] DATA LEDs show 004340 = 'HALT' shows R00
[X] DATA LEDs show 000000 = 'HALT' shows R0 in the current register
set
```

Movie: TB8A3133

Script 16 - BUS REGISTER SHOWS SWITCH REGISTER WHEN HALTED

Leave/set ENABLE/HALT at/to HALT (or leave CPU halted from script 15)
Switch the DATA knob to BUS REG
Play with the switches in the switch register to see if the switch settings are reflected in the DATA LEDs.

Movie: TB8A3134, invalid

Script 17 - EXAM/DEPOSIT Demo

Enter "Running light" per DEPOSIT over front panel

```
      1                                     .title  PDP-11/70 running light
      2                                     ; This program shihts endlessly a bit in R0
      3                                     ; and show each value on the DATA LEDs.
      4                                     ; Display time is given by RESET opcode.
      5                                     ; DATA_SELECT must be set to DISPLAY REG
      6
      7                                     ; "sim> set cpu 11/40"
      8
      9 177570                        dr    = 177570        ; switch/ display register
     10                                     .asect
     11 001000                              .=1000          ; program loads at 1000
     12
     13                               start1:
     14 001000 012701  177570               mov     #dr,r1
     15 001004 005000                       clr     r0      ; set bit 0 in R0
     16 001006 005200                       inc     r0      ;
     17                               loop1:
     18 001010 006100                       rol     r0
     19 001012 010011                       mov     r0,@r1  ; write to display register
     20 001014 000005                       reset           ; 70ms display pause
     21 001016 000774                       br      loop1
```

[ ] After LOAD ADRS, is really CONS PHY == PROG PHY?
[ ] EXAM on illegal address 776000   => ADRS ERR?

Verify by DEPOSIT

[ ] does LEDs flash on LOAD ADR? EXAM ? DEPOSIT ? NO

Run @ 1000
While running: ADDR select all 8 positions. DATA SEL all 4 positions.

Movie: TB8A3106

The running dot is much faster than expected, as on 11/70 RESET lasts only 10ms instead of 70ms.

Test 18 – Running an Unix 7th edition

Let LCM run their Unix 7th edition demo on the 11/70.

Watch lamps. Turn ADDR SEL and DATA SEL to all positions

What is µADDR FPP/CPU doing ?

[ ] video of booting: TB8A3135

[ ] video of idle (shell logged in) TB8A3136

[ ] video of heavy user CPU (

„cc prime.c“, DATA SEL in4 positions: TB8A3342,3,4,5

„a.out >/dev/null“ DATA SEL in 2 positions: TBA8A3346,7

[ ] video of heavy file system user CPU (du >/dev/null) TB8A3137

OBSERVATIONS

Observation 1 – CONS PHY

TB8A3109: The addresses shown when rotating the ADDR knob always show the same address (also for CONS PHY).

Explanation:

In the 11/70, there is no persistent „Console Address Register“, clocked by LOAD ADR. CONS PHY is split into two halves, see EK-KB11C-TM-001, page III-2-5.

Bits 15:00 are implemented by several data path register operations under microcode control, they are volatile. Despite labeled "PHY", the Display LEDs are driven by internal "Virtual Adress" lines.If the CPU is running, they show nonsense: a mix of "PROG VIRTUAL" and Switches 21:16.

Bits 21:16 are easy: taken from Switches, clocked by LOAD ADRS, persistent.

Bits 15:00 are saved in datapath SR register and displayed from MMU input virtual address (BA, BAMUX). Micro code is FPMS FLOWS 14 and 12. In HALT, always SR (=BAMUX) is visible on CONS PHY (uStep CON.00). LOAD ADRs clocks Switches (over BR) into SR (uStep ADR.00). On HALT, uStep FLOWS 12, BRK.00 copies Programcounter SR := PCB, and shows SR on Virtual address Lines BA (CON.00).

For display, CONS PHY connects the LEDs to virtual address 15:0, and Switch Reg 21:16 (EK-KB11C-TM-001, II-2.8/9/10). So on RUN the CONS PHY display is in fact internal virtual addresses, as all the VIRTUAL settings. PROG PHY shows physical addresses.

Consequences:

- EXAM STEP, DEP STEP only increments only Bits 15:00?
- Bits 15:00 of CONS PHY (SR register!) are changed by program execution, Single Step, and ADRS ERRS. Maybe ADR ERRs clears SR. TB8A3119 shows CONS PHY going to 17600000, as Switches 21:16 are 1s.

- Current PC in CONS PHY after Single Step/HALT (FLOWS 12 BRK.00) is virtual, but bits 21:16 are latched switch settings?
- Switches latched into Switch Register on LOAD_ADRS? Not more often? FPMS UBCF SCCH LOAD ADRS -> CNSL07 -> SCCK

Access to General Registers R00—R17 is implemented totally different.

See „KB11C PROCESSOR MANUAL (PDP-11-70) (1975, EK-KB11C-TM-001)“, pdf page 197. The CONS PHY display involves

„IN CON SPHY, the LEDs 0..15 show VA(00:15), leds 16:21 show SWR (16:21) … the Switches are read into SR (Source Register) on LOAD ADRS.“

SCCJ = 181, SCCK = pdp 182.

Observation 2 – ADRS ERS

TB8A3119: In the video, LOAD ADRS + EXAM of illegal address lights the ADRS ERR LED and also sets the ADRS LEDS to 17600000. Since the address 17600000 is valid (if you have 4MB memory) this behaviour seems very odd. REALCONS lights the ADRS ERR LED for the first illegal address but then seems to change the loaded address internally to 17600000 but not on the ADRS LEDs.

TB8A3121: EXAM from starting from 17777674 below the registers into the registers 17777700 lights the ADRS ERR LED correctly but changes the CONS PHY back to 17777674. Behaves like ADRS ERR generated a LOAD ADRs. After that an 4th EXAM on reloaded 17777674 has no effect.

Possible explanation:

Bits 15:00 of CONS PHY are implemented by datapath Register SR.

Bits 21:16 always reflect the LOAD ADR Switches.

Handling of UNIBUS timeout etc. may involve more micro code steps, deleting or changing SR and resulting in random display.

Observation 3 – Parity display

TB8A3109:

Parity_HIGH / _LOW is always visible, but makes only sense for DATA Selection = BUS REG.

In TB8A3106 an EXAM sequence is seen without PARITY display.

Maybe because that code was entered over Console DEPOSIT?

Observation 4 – USER/SUPER/KERNEL mode

TB8A3119:

When switching ENA/HALT to HALT while BLINKY is in either USER or SUPER mode, the mode LED is changed to KERNEL mode. I would expect it to stay in the current mode. The PSW reflects this change too (so the LED matches the PSW, I just think the PSW is incorrect). In the video, none of the KSU LEDs are on. In other videos one of KSU is lit even when RUN is off. Hard to say what the rules are.

Observation 5 - PAUSE

TB8A3135:

While booting Unix V7, RUN is very dim and PAUSE is bright.

This may be caused by a scan for memory, with lots of UNIBUS timeouts.

I think nothing can be done here, SimH does not emulate UNIBUS timing.