MODCOMP Classic

Josh Heaton

History

The MODCOMP Classic was built by MODCOMP (Modular Computer Systems, Inc) in 1978. The Classic replaced the MODCOMP IV, offering full support for 32-bit addressing. The platform offered 240 general purpose registers, addressable as 16 banks of 15 registers. The machine also had a special register zero that reflected the state of the data switches on the front panel.

MODCOMP was popular in process control applications, offering deterministic real-time interrupts and real-time control. The architecture was modular in nature (hence the name), allowing systems to be built to match the intended application. The system was even adopted by NASA, tracking space probes and collecting data and ultimately controlling the Space Shuttle launch at Cape Canaveral.

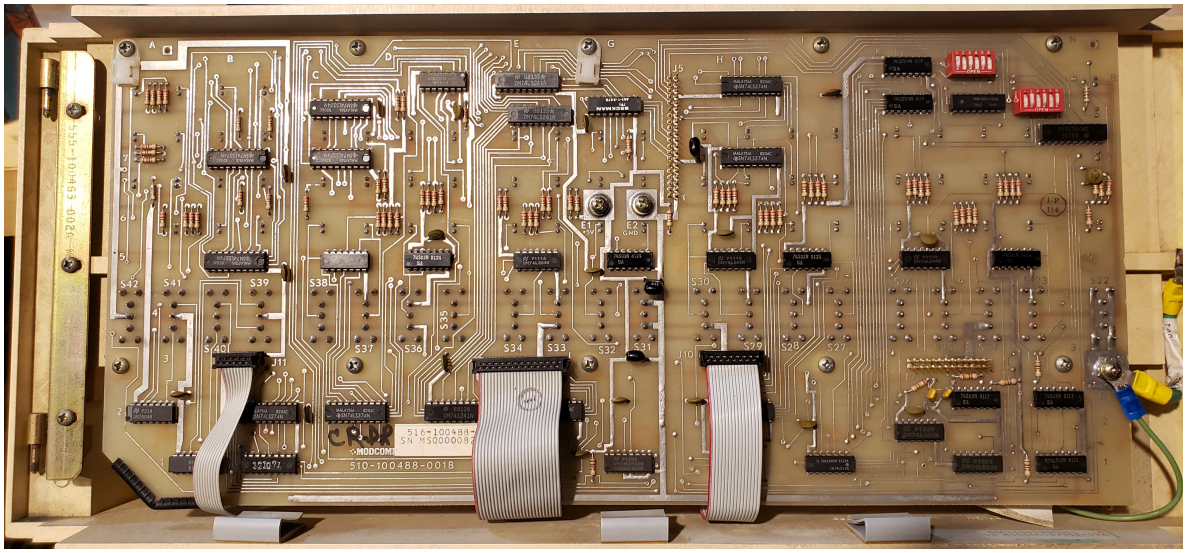
The MODCOMP was somewhat unique in that it had a phased clock signal. The full fetch/decode/execute/store cycle was completed with each CPU clock. So for example, the 7850 had a CPU frequency of 66 MHz and was capable of 66 MIPS.

7830 Control Panel

The Model 7830 had a control panel with 16 data switches (that set the value in register 0), the ability to step the processor one instruction at a time, and inspect/modify any value in memory at any point in time. A security key disables the HALT/RUN switch for an extra layer of physical protection in critical applications. MODCOMP panels were tied directly to the CPU, so panels could not be swapped between different models.

The panel itself operates with an 8-bit bi-directional data bus and 3-bit address bus. There are also several bus pins dedicated to hard-wired switches such as halt, master clear, and console interrupt. The entire panel runs on 5VDC, consuming approximately 1500mA of current.

All of the panel's functionality is accessible through a 40 pin header, "J5". Half of J5 is tied to ground, leaving only 20 true I/O pins. Save for one chip, all of the logic is stock 74LS-series. Ground is logic TRUE.



I/O Map

The pin mapping of J5 is as follows:

Pin	Direction	Function	Pin	Direction	Function
40	O	BP-HLT Switch Output	39	-	Ground
38	O	CSL INT (Console Interrupt) Output	37	-	Ground
36	O	M CLEAR Switch Output	35	-	Ground
34	O	HALT Switch Output	33	-	Ground
32	I	STANDBY LED Input (+5VDC)	31	-	Ground
30	I	READ (H) / WRITE (L)	29	-	Ground
28	I	STANDBY	27	-	Ground
26	I	BACKUP FAILURE	25	-	Ground
24	I	Clock	23	-	Ground
22	I	Address Bit 1	21	-	Ground
20	I	Address Bit 2	19	-	Ground
18	I	Address Bit 0	17	-	Ground
16	I/O	Bit 7	15	-	Ground
14	I/O	Bit 6	13	-	Ground
12	I/O	Bit 4	11	-	Ground
10	I/O	Bit 5	9	-	Ground
8	I/O	Bit 0	7	-	Ground
6	I/O	Bit 1	5	-	Ground
4	I/O	Bit 2	3	-	Ground
2	I/O	Bit 3	1	-	Ground

Registers

As indicated by the address lines, the panel is mapped into 16 logical registers (8 readable, 8 writable). The writable registers are fairly straight-forward:

Address	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	Low Byte of Address							
1	High Byte of Address							
2	Low Byte of Data							
3	High Byte of Data							
4	II PROT	PRIV	I/O	TASK	EMA 1	EMA 2	EMA 3	EMA 4
5	VM	PM	MERR	RUN	N	Z	O	C
6	Not Used							
7	Writing this address will clock in all switch inputs							

Note special register 7. The CPU writes this register (value is discarded) to latch in all switches into each 74LS374. This must be done BEFORE reading any of the registers. The readable registers are a bit more convoluted:

Address	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	High Byte of Data Switches							
1	High Byte of Data Switches							
2	Low Byte of Data Switches							
3	High Byte of Data Switches							
4	HALT State, see below				MEM	INTS	PSW	ISTK
5	IOP	MBC	CTXT	MAP	EAU	EAU	CPU	CPU
6	IOP	MBC	CTXT	MAP	EAU	EAU	CPU	CPU
7	IOP	MBC	CTXT	MAP	EAU	EAU	CPU	CPU

Halt State

Note that some registers are duplicated due to the panel using logic gates for selecting which chips to read from. Of note is register 4. When the HALT switch is active, the lower 4 bits of that register drive several operations for entering values into memory:

Switch	Bit 0	Bit 1	Bit 2	Bit 3	Notes
SGL STP	0	0	0	0	Single step
ENT NXT	1	0	0	0	Virtual, Oper mode
ENT NXT	0	1	0	0	Actual, Inst mode
ENT NXT	1	1	0	0	Virtual, Inst mode
None	0	0	1	0	No switch pressed
ENT P/MA	1	0	1	0	Virtual mode
ENT P/MA	0	1	1	0	Actual mode
FILL	0	0	0	1	Fill switch pressed, loads ROM code into low memory
ENT MEM	1	0	0	1	Virtual, Oper mode
ENT MEM	0	1	0	1	Actual Inst, Actual Oper mode
ENT MEM	1	1	0	1	Virtual Inst mode
ENT REG	0	0	1	1	
STP P/MA	1	0	1	1	Virtual mode
STP P/MA	0	1	1	1	Actual mode

Signal Sequencing for Write

1. Clock must be high
2. Set R/W low
3. Set address
4. Set data
5. Strobe clock low, pulling back high again

Signal Sequencing for Read

1. Clock must be high
2. Set R/W high
3. Set address
4. Pull clock low
5. Wait approx. 1ms (could be less, have not determined exact timing)
6. Read data
7. Set clock high