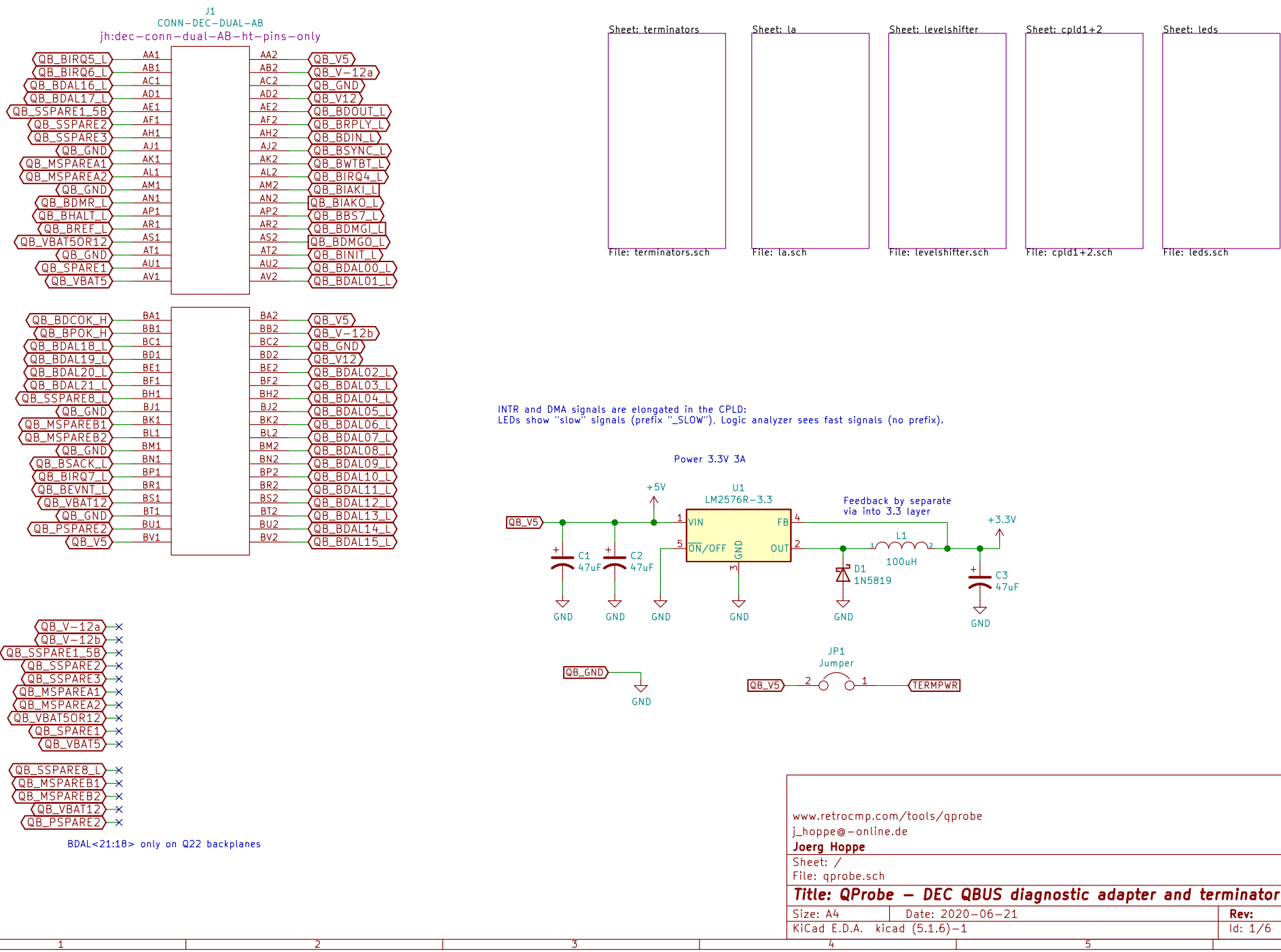
J1
CONN-DEC-DUAL-AB
jh:dec-conn-dual-AB-ht-pins-only
QB_BIRQ5_L AA1
QB_BIRQ6_L AB1
QB_BDAL16_L AC1
QB_BDAL17_L AD1
QB_SSPARE1_5B AE1
QB_SSPARE2 AF1
QB_SSPARE3 AH1
QB_GND AJ1
QB_MSPAREA1 AK1
QB_MSPAREA2 AL1
QB_GND AM1
QB_BDMR_L AN1
QB_BHALT_L AP1
QB_BREF_L AR1
QB_VBAT5OR12 AS1
QB_GND AT1
QB_SPARE1 AU1
QB_VBAT5 AV1
AA2 QB_V5
AB2 QB_V-12a
AC2 QB_GND
AD2 QB_V12
AE2 QB_BDOUT_L
AF2 QB_BRPLY_L
AH2 QB_BDIN_L
AJ2 QB_BSYNC_L
AK2 QB_BWTBT_L
AL2 QB_BIRQ4_L
AM2 QB_BIAKI_L
AN2 QB_BIAKO_L
AP2 QB_BBS7_L
AR2 QB_BDMGI_L
AS2 QB_BDMGO_L
AT2 QB_BINIT_L
AU2 QB_BDAL00_L
AV2 QB_BDAL01_L
QB_BDCOK_H BA1
QB_BPOK_H BB1
QB_BDAL18_L BC1
QB_BDAL19_L BD1
QB_BDAL20_L BE1
QB_BDAL21_L BF1
QB_SSPARE8_L BH1
QB_GND BJ1
QB_MSPAREB1 BK1
QB_MSPAREB2 BL1
QB_GND BM1
QB_BSACK_L BN1
QB_BIRQ7_L BP1
QB_BEVNT_L BR1
QB_VBAT12 BS1
QB_GND BT1
QB_PSPARE2 BU1
QB_V5 BV1
BA2 QB_V5
BB2 QB_V-12b
BC2 QB_GND
BD2 QB_V12
BE2 QB_BDAL02_L
BF2 QB_BDAL03_L
BH2 QB_BDAL04_L
BJ2 QB_BDAL05_L
BK2 QB_BDAL06_L
BL2 QB_BDAL07_L
BM2 QB_BDAL08_L
BN2 QB_BDAL09_L
BP2 QB_BDAL10_L
BR2 QB_BDAL11_L
BS2 QB_BDAL12_L
BT2 QB_BDAL13_L
BU2 QB_BDAL14_L
BV2 QB_BDAL15_L
QB_V-12a
QB_V-12b
QB_SSPARE1_5B
QB_SSPARE2
QB_SSPARE3
QB_MSPAREA1
QB_MSPAREA2
QB_VBAT5OR12
QB_SPARE1
QB_VBAT5
QB_SSPARE8_L
QB_MSPAREB1
QB_MSPAREB2
QB_VBAT12
QB_PSPARE2
BDAL<21:18> only on Q22 backplanes
Sheet: terminators
File: terminators.sch
Sheet: la
File: la.sch
Sheet: levelshifter
File: levelshifter.sch
Sheet: cpld1+2
File: cpld1+2.sch
Sheet: leds
File: leds.sch
INTR and DMA signals are elongated in the CPLD:
LEDs show "slow" signals (prefix "_SLOW"). Logic analyzer sees fast signals (no prefix).
Power 3.3V 3A
+5V
U1
LM2576R-3.3
VIN
ON/OFF
GND
FB
OUT
Feedback by separate
via into 3.3 layer
+3.3V
L1
100uH
D1
1N5819
C1
47uF
C2
47uF
C3
47uF
GND
QB_V5
QB_GND
JP1
Jumper
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Sheet: /
File: qprobe.sch
Title: QProbe – DEC QBUS diagnostic adapter and terminator
Size: A4
Date: 2020-06-21
Rev:
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CPLD1 LEDs:
11x ADR<10:00>
11x DAT<10:00>
=> 11 per I/O Bank

"_" signal prefix = signal generated by CPLD

CPLD2 LEDs:
11x ADR<21:11>
5x DAT<15:11>
8x _SLOW IRQ4,5,6,7,IAK,DMR,DMG,SACK
=> 12 per I/O Bank

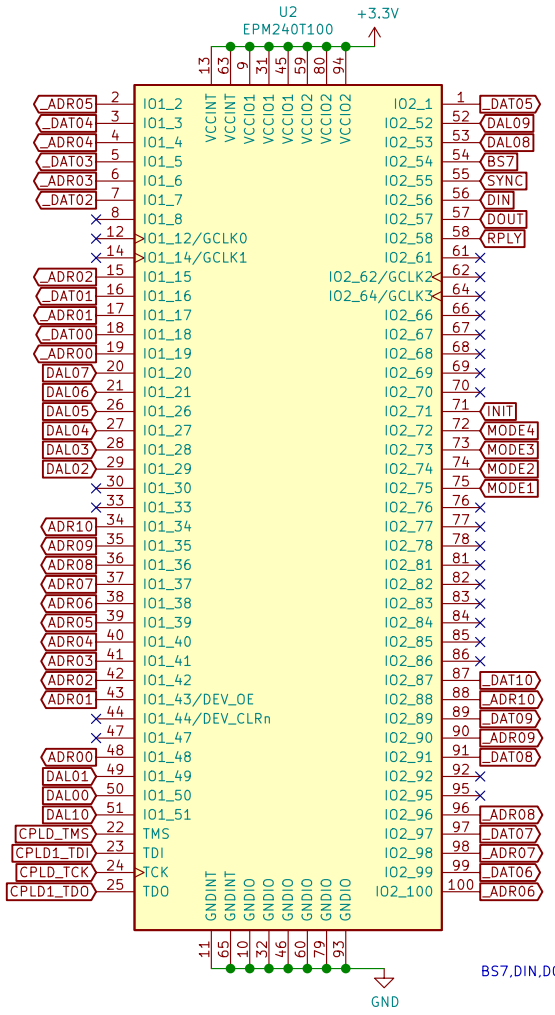
LED driver current limits:

Application Note AN286: "MAX II EPM240 as LED driver"
LED 10mA max.

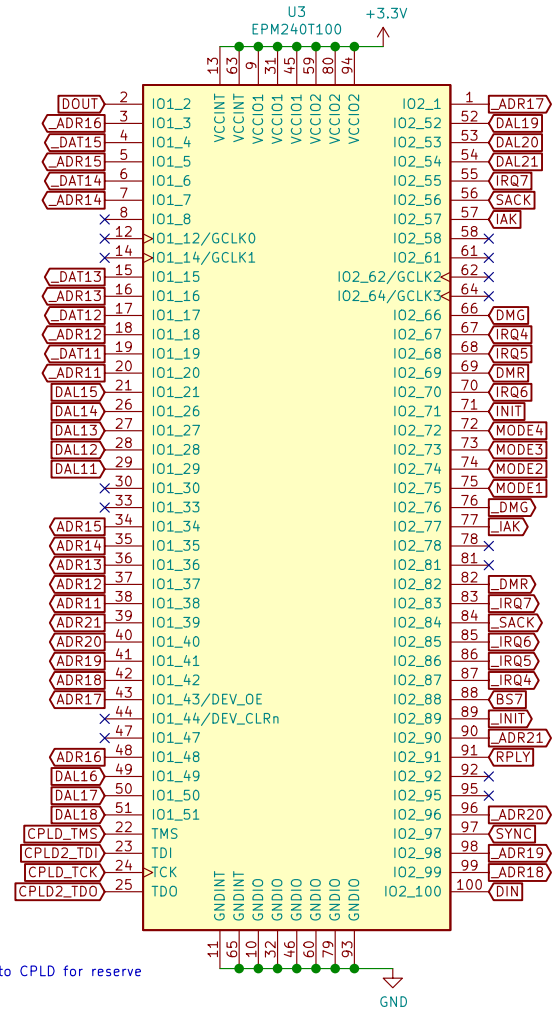
a) EPM240: 25mA per pin -> OK

b) Total load:
Source per "VCCIO group": 170 mA
Sink per "GNDIO group": 130 mA
6 VCCIO pins => 6*130 = 0.78 A ?
Not clear how pins are assigned to "GNDIO regions".
=> assume 130mA per IO BANK, or a bit more.

To drive by CPLD (others driven by 74LVC245):
ADR<21..00>, DAT<15..0>, 8x"INTR/DMA => 46 LEDs
=> 460mA = 4 Banks with 115mA => 2 CPLDs needed.

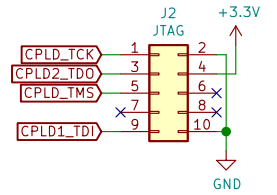


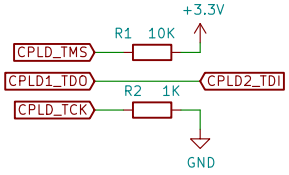
Pins adjacent to PWR/GND:
8
12
14
30
33
44
47
58
61
62
64
66
78
81
92
95

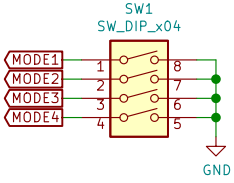


BS7,DIN,DOUT,RPLY routed in to CPLD for reserve

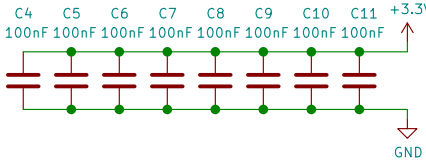
JTAG chain:
TDI1-PLD1-DO1 -> TDI2-CPLD2-TDO2

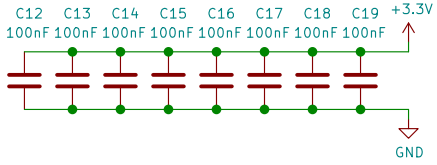






In CPLD enable "weak pull up resistors" on pin (range 50k-100k)





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Sheet: /cpld1+2/
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Title: QProbe - DEC QBUS diagnostic adapter and terminator

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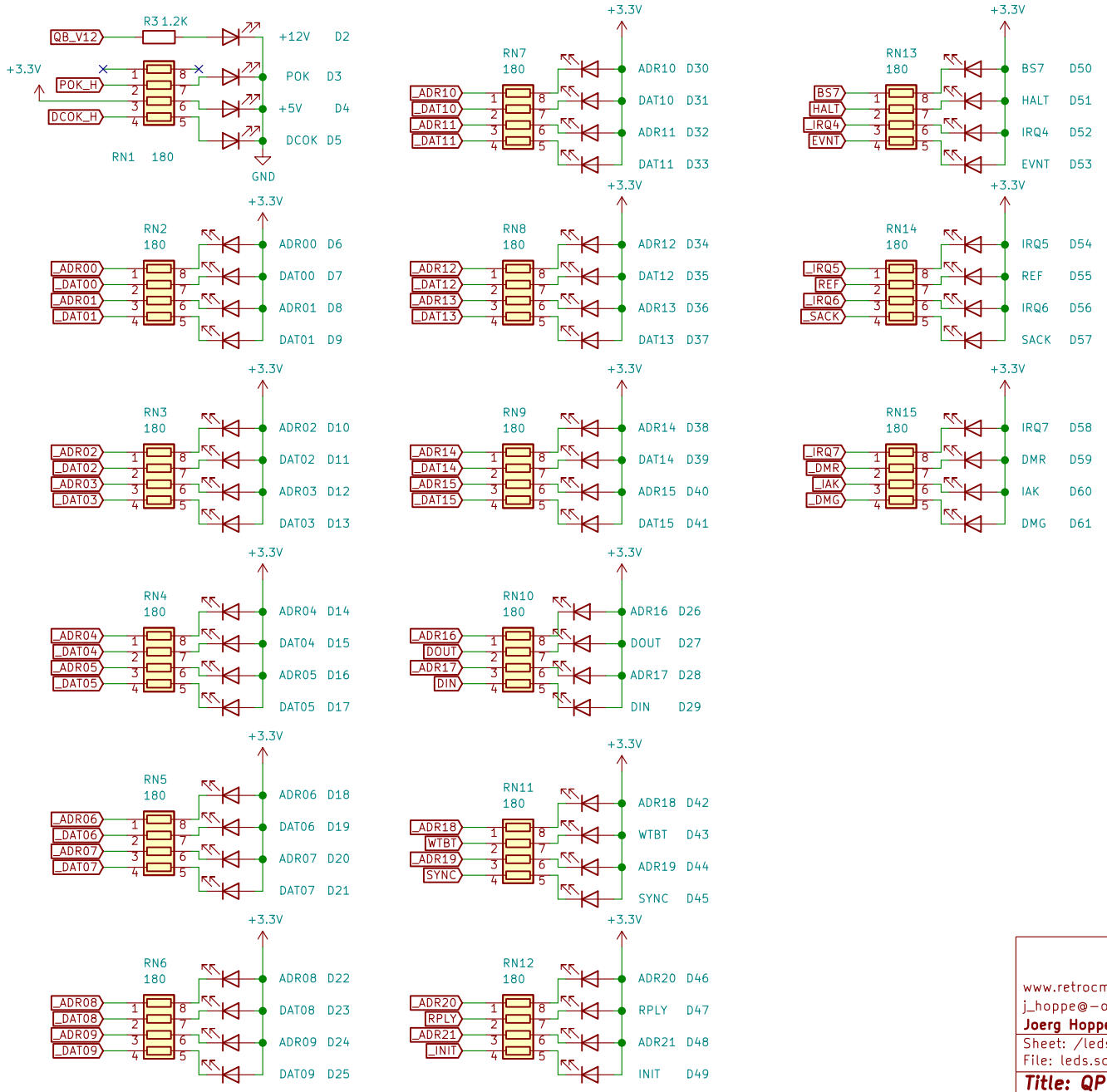
All input except POK and DCOK inverted. "_" signal prefix = LED signal generated by CPLD



LED current:
must be < 10mA.
74LCV245 can drive max 5 LEDs à 10mA.
CPLD driving limit:
Test at 3.4V
Reichelt LED 3MM RT: R=150, I=8.7 mA
Reichelt LED 3MM GE RT: R=150, I=9.3 mA
Reichelt LED 3MM GN RT: R=150, I=8.8 mA

Power calculation (150Ohm)

Psingle = I^2*R = 0.0087^2*150 = 11mW
Ppack = 4*Psingle = 44mW
Prated (70°) = "1/16W" = 62mW => OK

LED current:
Test at 5.1V, Reichelt LED 3MM RT:
R=330, I=9.4mA
R=360, I=8.5mA

Test at 12V, Reichelt LED 3MM RT:
R=1.0k, I=10.0mA
R=1.2k, I=8.5mA

P = I^2R = 0.0085^2*1200 = 86mW
Pmax (case 0805) = 125mW

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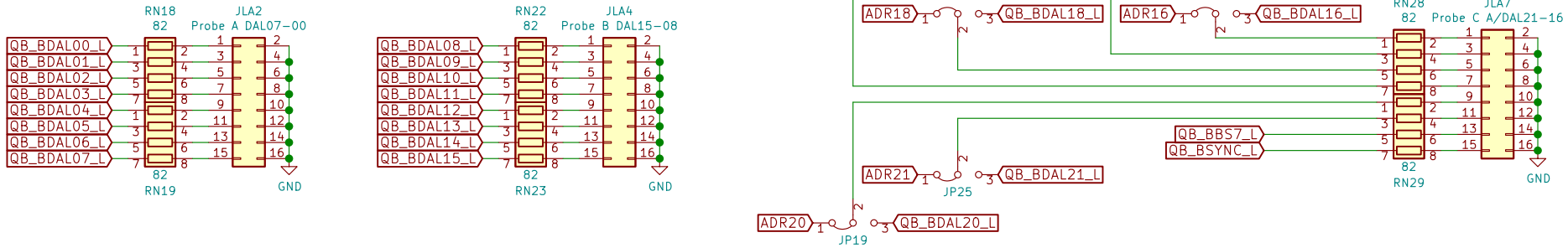
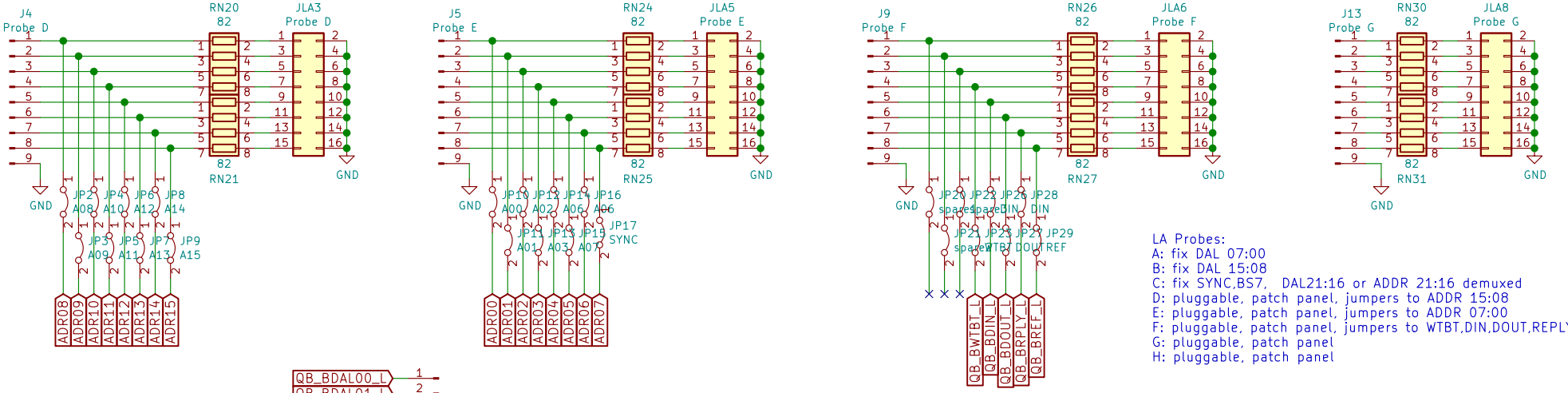
Inline terminators before LA probes
inhibit signal reflection & bounce.
82 ohm for 50cm Zeroplus flat cable

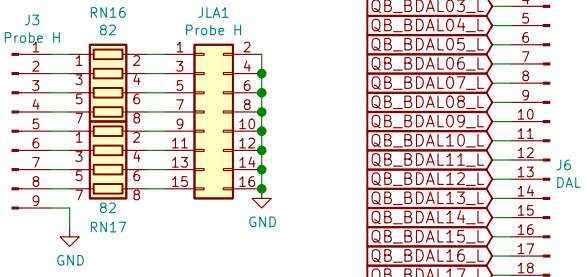
All signals inverted, expcept POK and DCOK.

DATA shows DAL, ADR latched by CPLD.



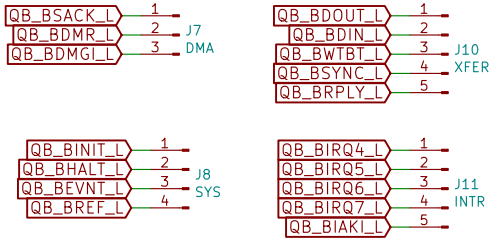


LA Probes:
A: fix DAL 07:00
B: fix DAL 15:08
C: fix SYNC,BS7, DAL21:16 or ADDR 21:16 demuxed
D: pluggable, patch panel, jumpers to ADDR 15:08
E: pluggable, patch panel, jumpers to ADDR 07:00
F: pluggable, patch panel, jumpers to WTBT,DIN,DOUT,REPLY,REF
G: pluggable, patch panel
H: pluggable, patch panel



LA bread board connectors same visible order as LEDs

ATTENTION:
Some LED signals (IRQ, GRANT, ...) are slowed for human eye.
Logc Analyzer interface connects "fast" signals.



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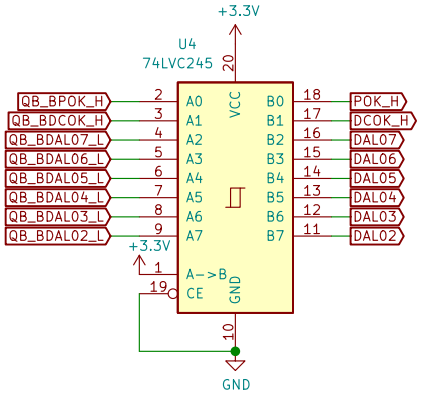
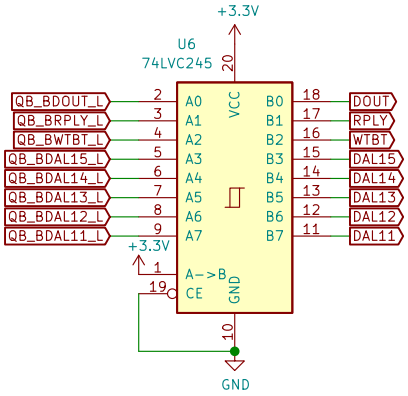
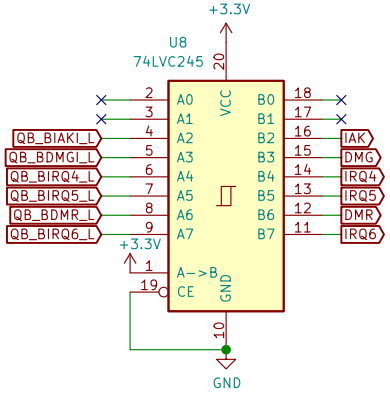
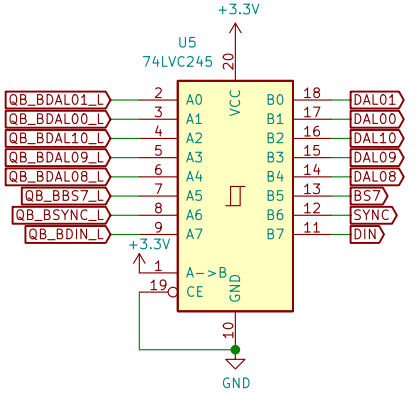
74LVC245: can drive 50mA => connect only 5 direct driven LEDs

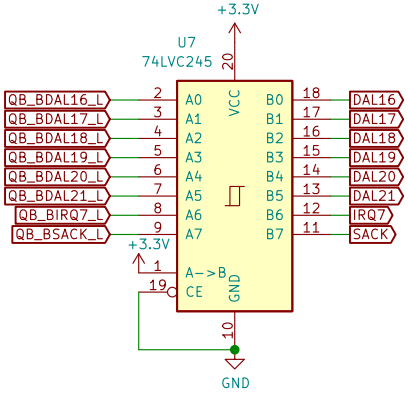
Driven LEDs: (not delayed by CLPLDs): POK, DCOK, WTBT, DIN, DOUT, SYNC, RPLY, REF. BS7, HALT, EVNT

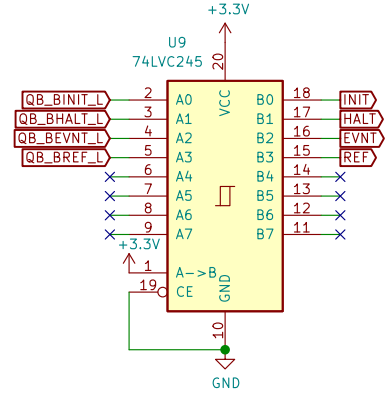


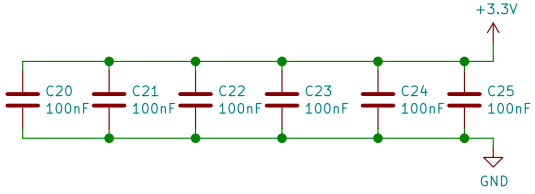












Sheet: /levelshifter/
File: levelshifter.sch

Title:

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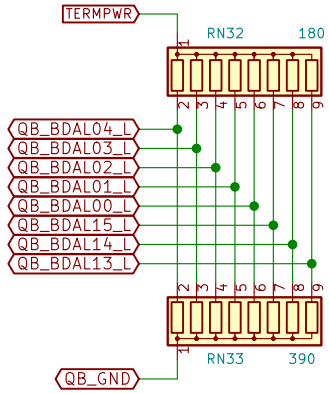
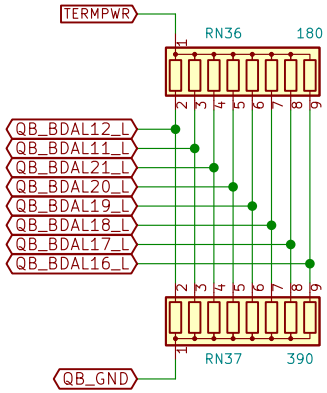
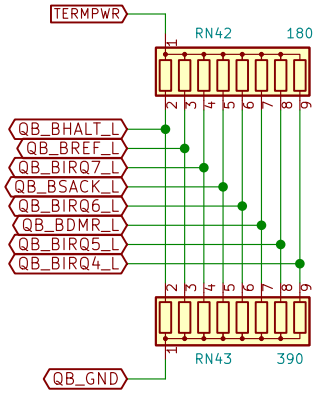
Terminator impedance maybe "open", 120 or 240 Ohm, see http://web.frainresearch.org:8080/projects/pdp-11/backplanes.php

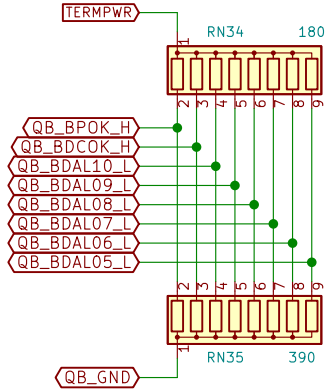
"A system with a 240 ohm processor can accommodate up to 20 AC loads, without far end termination.
A system with a 240 ohm processor can accommodate up to 35 AC loads, with 240 ohm termination on the far end. The far end termination may also be 120 ohms, but this is considered to be less optimal.
A system with a 120 ohm processor can accommodate up to 35 AC loads, without far end termination.
A system with a 120 ohm processor can accommodate up to 45 AC loads, with 120 ohm termination on the far end."

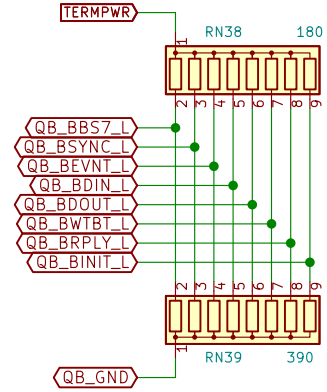
120 Ohm (default) with 180/390, see BDV11AA M8012. 220 ohm with 330/680, see LSI11/03 M7264.

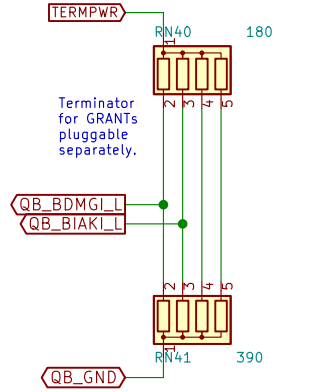


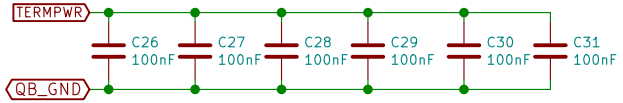




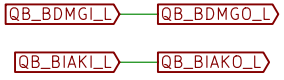








GRANT continuity forwarded



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